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Case No. IPR2014-00564
**Chrysler Group LLC v. Norman IP Holdings, LLC**

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Paper 18
Entered: September 23, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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NISSAN NORTH AMERICA, INC.,
Petitioner,

v.

NORMAN IP HOLDINGS, LLC,
Patent Owner.

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Case IPR2014-00564
Patent 5,530,597

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Before BRYAN F. MOORE, HYUN J. JUNG, and
FRANCES L. IPPOLITO, *Administrative Patent Judges.*

IPPOLITO, *Administrative Patent Judge.*

# DECISION
Institution of *Inter Partes* Review
*37 C.F.R. § 42.108*

## I. INTRODUCTION

Nissan North America, Inc.[1] ("Petitioner") filed a Petition ("Pet.") on April 1, 2014, requesting an *inter partes* review of claims 6–9 of U.S. Patent No. 5,530,597 ("the '597 patent"). Paper 1. Patent Owner Norman IP Holdings, LLC waived the Preliminary Response to the Petition. Paper 7.

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

Pursuant to 35 U.S.C. § 314, we conclude there is a reasonable likelihood that Petitioner would prevail with respect to claims 6–9 of the '597 patent.

### *A. Related Proceedings*

Claims 1–6, 10, and 11 of the '597 patent were the subject of *Ex Parte* Reexamination No. 90/012,781, filed on February 4, 2013. Ex. 1010, 2, 5. This reexamination resulted in *Ex Parte* Reexamination 5,530,597 Certificate C1, issued April 17, 2014 ("'597 C1"), indicating that claims 1–5, 10, and 11 were cancelled, the patentability of claim 6 was confirmed, and claims 7–9 were not reexamined. Ex. 3001.

Claims 1–6, 10, and 11 of the '597 patent were also the subject of a request for a second *Ex Parte* Reexamination No. 90/012,901, filed by third

[1] Chrysler Group LLC was originally listed with Nissan North America, Inc. as Petitioner in the Petition. Pet. 1. Subsequently, Chrysler Group LLC and Patent Owner Norman IP Holdings, LLC jointly moved to terminate the proceedings as to Chrylser Group LLC only. Paper 9. We granted the motion on August 25, 2014. Paper 13. Thus, Nissan North America, Inc. remains as the only Petitioner in this proceeding.

party requestor ARM, Inc. on June 27, 2013. That request was denied on August 27, 2013. Ex. 1010, 3–4. Third party requestor ARM, Inc. filed a Petition for review of the denial on September 25, 2013. On April 23, 2014, ARM, Inc.'s Petition for review was dismissed as moot in view of the '597 C1. Ex. 3002.

For other related proceedings, Petitioner provides a list of related matters in various federal district courts. Pet. 2–5.

*B. The '597 Patent*

The '597 patent describes interrupt controllers with interrupts that may be masked by software. Ex. 1001, 1:54–56. More particularly, the '597 patent describes an interrupt enable circuit "capable of allowing an interrupt to be enabled and disabled by software at any time except under conditions, dictated by hardware, at which time the interrupt becomes non-maskable." *Id.* at 3:9–12. Figure 2 of the '597 patent is reproduced below.

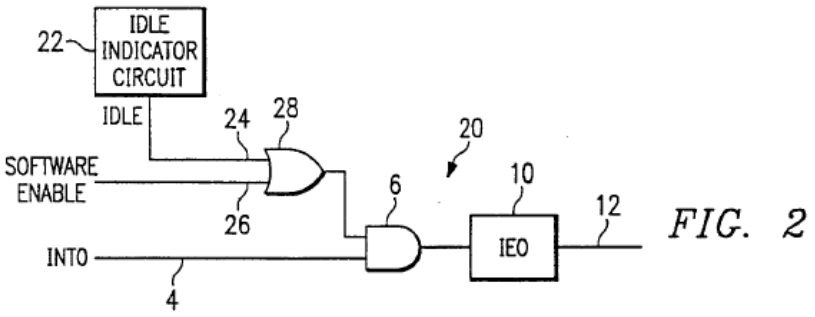



FIG. 2

Figure 2 depicts an interrupt enable circuit that provides a maskable interrupt that becomes a "non-maskable interrupt while the processor is in the idle mode." *Id.* at 5:49–52. Generally, when the SOFTWARE ENABLE signal is high, the interrupt request signal, INTO, will generate an interrupt. *Id*. at 5:21–23. When the SOFTWARE ENABLE signal is low, the interrupt is

masked. *Id.* at 5:24–25. However, IDLE INDICATOR CIRCUIT 22 provides an IDLE signal on line 24 while the processor is in idle mode. *Id.* at 5:54–56. The IDLE signal is received with the SOFTWARE ENABLE signal by OR gate 28. *Id.* at 5:56–57. Thus, when the processor is in an idle mode, IDLE INDICATOR CIRCUIT 22 will assert an IDLE signal and cause the output of OR gate 28 to go high regardless of the state of the SOFTWARE ENABLE signal on line 26. *Id.* at 5:61–65. "As long as the OR gate output 28 remains at a high level . . . [the] INTO [signal] on line 4 will set latch 10, thus generating the interrupt." *Id.* at 5:65–6:1. When the processor is not in the idle mode, the IDLE signal on line 24 remains low, and the enabling and disabling of the interrupt will be determined by the SOFTWARE ENABLE signal on line 26. *Id.* at 6:7–10.

### *C. Illustrative Claim*

Challenged claims 6–9 depend directly or indirectly from claims 1, 4, and/or 5, which were cancelled by the *Ex Parte* Reexamination No. 90/012,781. Illustrative claim 6 and cancelled claims 1, 4, and 5 are reproduced below:

> 1. (Cancelled) An interrupt mask disable circuit comprising:
>
> first logic circuitry operably coupled to receive an interrupt request and a mask signal and to provide an interrupt signal when the interrupt request is active and the mask signal is disabled, and to provide a non-interrupt signal when the mask signal is enabled regardless of whether the interrupt request is active or inactive; and
>
> second logic circuitry operably coupled to receive a mask activation signal and a mask override signal and to produce the mask signal, wherein the mask signal is enabled when the mask activation signal is active and the mask override signal is not enabled and wherein the mask signal is disabled

when the mask override signal is active regardless of whether the mask activation signal is enabled or disabled.

4. (Cancelled) The interrupt mask disable circuit of claim 1, wherein the mask override signal is enabled based on a hardware condition.

5. (Cancelled) The interrupt mask disable circuit of claim 4, further comprises being incorporated within a processor, and wherein the hardware condition occurs when said processor is in a particular state.

6. An apparatus as recited in claim 5 wherein said particular state comprises an idle mode.

*D. The Prior Art*

Petitioner relies on the following prior art:

1. U.S. Patent No. 4,748,559, issued May 31, 1988 ("Smith") (Ex. 1004);
2. U.S. Patent No. 4,930,068, issued May 29, 1990 ("Katayose") (Ex. 1003);
3. Japanese Pub. S61-39135, published Feb. 25, 1986 ("Tokiwa") (Ex. 1002);
4. *MSM80C154S MSM83C154S MSM85C154HVS USER'S MANUAL*, OKI Electric Industry Company, Ltd. (1988) ("OKI") (Ex. 1005); and
5. *1990 Single-Chip Microcontroller Data Book*, NEC Electronics Inc. (May 1990) ("NEC") (Ex. 1006).

*E. The Asserted Grounds*

Petitioner asserts that the challenged claims are unpatentable based on the following grounds:

| **Reference[s]** | **Basis** | **Claims Challenged** |
|---|---|---|
| Tokiwa[2] and Smith | § 103 | 6–9 |
| Katayose and Smith | § 103 | 6–9 |
| Smith | § 103 | 6–7 |
| Smith | § 102 | 6–7 |
| NEC | § 102 | 6–7 |
| OKI | § 102 | 6–7 |

## II. ANALYSIS

### *A. Claim Construction*

The '597 patent appears to be expired. *See* Pet. 8. The Board's review of the claims of an expired patent is similar to that of a district court's review. *In re Rambus Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012). We are, therefore, guided by the principle that the words of a claim "are generally given their ordinary and customary meaning" as understood by a person of ordinary skill in the art in question at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc) (internal citation omitted). For purposes of this decision, we need not expressly construe any term.

[2] We refer to "Tokiwa" as the English translation of the original reference, which Petitioner provided in the same exhibit as the original reference.

*B. Claims 6–9 – Obviousness over Tokiwa and Smith*

Petitioner argues that claims 6–9 are unpatentable under 35 U.S.C. § 103(a) over Tokiwa and Smith. Pet. 9–20. We have considered the arguments and evidence presented, and conclude that Petitioner has established a reasonable likelihood of prevailing on this ground.

*1. Summary of Tokiwa (Ex. 1002)*

Tokiwa teaches a virtual machine system with a virtual machine control program (VMCP) that manages machine resources shared among virtual machines (VM). VMCP operates in a privileged mode and the operating system (OS) under the VM operates in a non-privileged status or privileged status. Ex. 1002, 2. "Direct execution of privileged commands and interrupts on the VM means that privileged commands or interrupts belonging to the VM are executed in nearly the same execution time as in the actual machine, primarily by hardware." *Id.* at 3.

Tokiwa also discloses an interrupt processing mechanism to prevent a VM in standby uninterruptible state rendering the actual machine itself uninterruptible. Ex. 1002, 4. Figure 1, reproduced below, is a logic circuit diagram illustrating an interval timer interrupt processing mechanism for this purpose.

FIG. 1

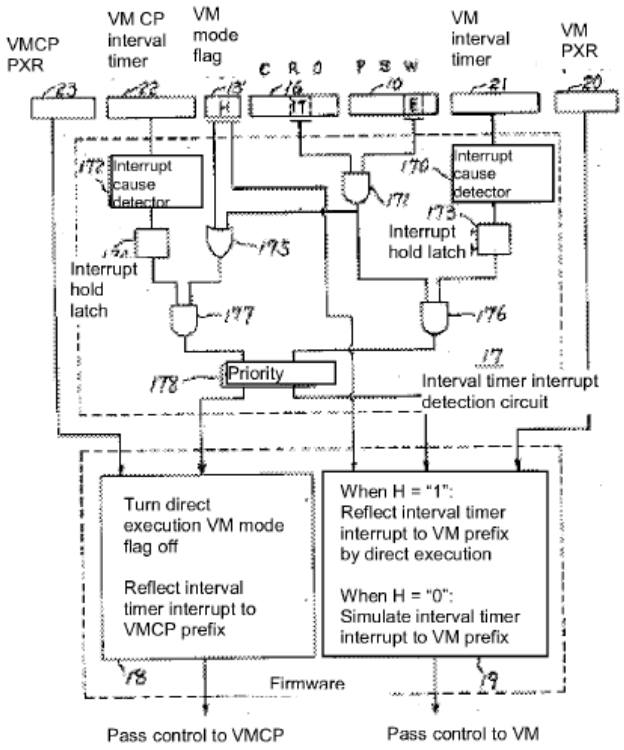



Figure 1 shows that the interval timer interrupt processing mechanism may include VM mode flag 13. VM mode flag 13 has a value of "1" when in VM mode and a value of "0" when in hypervisor (HPV) mode. Ex. 1002, 3. In VM mode, privileged commands can be executed by the VM. *Id.*

Figure 1 also shows interval timer interrupt detection circuit 17 that includes interrupt cause detection circuit 170 for VM interval timer 21, interrupt cause detection circuit 172 for VMCP interval timer 22, AND circuits 171, 176, and 177, and OR circuit 175 for processing the output of these interrupt cause detection circuits according to the contents of the external interrupt mask (E) of PSW 10, and the interval timer interrupt submask (IT) of CRO 16. *Id.* at 4.

Referring to Figure 1, Tokiwa describes the operation of the interrupt processing mechanism where an interrupt is generated by VMCP interval timer 22 while the direct execution mode of VM is running. In particular, Tokiwa states

> [i]n this case, "1" is output from the interrupt cause detection circuit 172. Since the direct execution VM mode flag 13' is "1," the output of the OR circuit 175 is "1," and as a result, the output of the AND circuit 177 is "1," and the VMCP interrupt processing firmware 18 is started up. The firmware 18 sets the value of the direct execution VM mode flag 13' to "0," and reflects the interval timer interrupt to the VMCP prefix indicated by the VMCP prefix register 23. That is, in this case, *when an interrupt cause is generated by the VMCP interval timer, the VMCP always performs interrupt, regardless of the contents of the interrupt masks (E and IT) (in this case these are used for the running VM).*

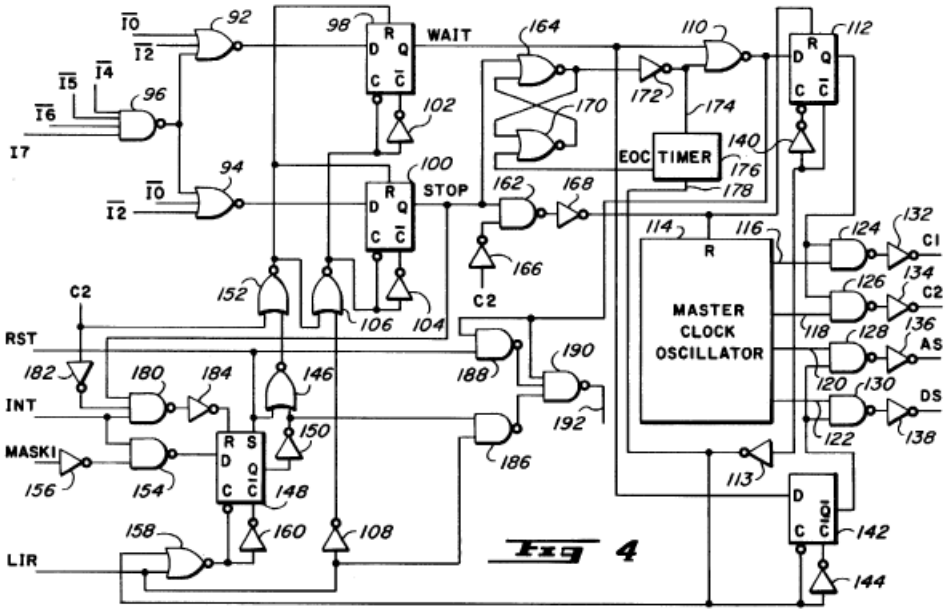
Ex. 1002, 4 (emphasis added). Tokiwa further discloses a second example where an interrupt is generated by VMCP interval timer 22 while the VM is not in direct execution mode. In the second example, VM mode flag 13' is "0" from the start. *Id.* at 5. In this mode, the interrupt is possible only when both the E (external interrupt mask) bit of the PSW 10 and the IT (interval timer interrupt submask) bit of CRO 16 are '1,' and the output of AND circuit 171 is '1.' *Id.* This results in an output of "1" from OR circuit 175 and an output of "1" from AND circuit 177. *Id.*

*2. Summary of Smith (Ex.1004)*

Smith discloses a processor capable of reducing its power consumption by executing a WAIT or STOP instruction. In either the WAIT or STOP state, the processor again is rendered operational or restarted by an external reset or the presence of an interrupt signal. Ex. 1004, 5:25–40,

Figs. 2–3 (flow diagrams showing execution of WAIT and STOP instructions). When a STOP instruction is executed, both the master clock oscillator and internal clocks are inhibited. *Id.* at 5:35–37.

Figure 4, reproduced below, is a logic diagram illustrating an apparatus for inhibiting clock signal in response to the WAIT or STOP instructions of Figures 2 and 3 to reduce power consumption in the processor.




As shown, Figure 4 depicts a logic diagram illustrating the WAIT instruction, STOP instruction, a reset signal (RST), an interrupt signal (INT), and a mask interrupt signal (MASK1). For masking, Smith further discloses that the processor includes a five-bit condition code register in which a "fourth bit is a mask interrupt bit and when set, disables both external and timer interrupts. Clearing the interrupt mask bit enables both of the interrupts." *Id.* at 3:22–25.

Referring back to Figure 4, Smith indicates that in WAIT mode, the

presence of an INT signal and in the absence of a MASK1 signal will result in a logical "0" applied to the D input of flip-flop 148. Ex. 1004, 7:29–32. This, in turn, will result in a logical "1" applied to the reset input of WAIT flip-flop 98, which enables clock signals C1 and C2 and address and data strobe signals AS and DS. *Id.* at 7:43–48. If an interrupt signal should occur after executing a STOP instruction, then flip-flop 148 must be reset asynchronously because master clock oscillator 114 has been disabled. Ex. 1004, 8:48–53. Smith adds that resetting flip-flop 148

> is accomplished as follows, a logical "1" on the interrupt input is applied to a first input of NAND gate 180. Since clock signal C2 is at a logical "0", a logical "1" is applied to a second input of NAND gate 180 via inverter 182. Finally, a third input of NAND gate 182 is coupled to the output of STOP flip-flop 100 which, after execution of the STOP instruction, is at a logical "1" level. Therefore, the output of NAND gate 180 is at a logical "0" level. This output is inverted by inverter 184 and applied to the R input of flip-flop 148.

*Id.* at 8:53–63.

*3. Analysis*

Below we discuss claim 6, which is illustrative of claims 7–9. Our discussion of claim 6 includes the limitations recited in cancelled claims 1, 4, and 5, which are required in dependent claim 6.

Cancelled claim 1 is directed to an interrupt mask disable circuit with

> first logic circuitry operably coupled to receive an interrupt request and a mask signal and to provide an interrupt signal when the interrupt request is active and the mask signal is disabled, and to provide a non-interrupt signal when the mask signal is enabled regardless of whether the interrupt request is active or inactive.

Petitioner asserts that Tokiwa's disclosure of the interval timer interrupt

processing mechanism, depicted in Figure 1's logic diagram, satisfies this limitation. Pet. 13–14. Specifically, Petitioner argues that Tokiwa provides an example where an interrupt cause is generated by the VMCP interval timer while the VM is not running in direct execution mode. *Id.* In that case, "interrupt is possible only when both the E (external interrupt mask) bit of the PSW 10 and the IT (interval timer interrupt submask) bit of the CRO 16 are '1.'" *Id.* (citing Ex. 1002, 5). Based on the current record, we are persuaded by Petitioner that Tokiwa's interval timer interrupt processing mechanism discloses the recited first logic circuitry with the required interrupt request (i.e., interrupt cause) and mask signal (i.e., E and IT masks).

Cancelled claim 1 further requires a

> second logic circuitry operably coupled to receive a mask activation signal and a mask override signal and to produce the mask signal, wherein the mask signal is enabled when the mask activation signal is active and the mask override signal is not enabled and wherein the mask signal is disabled when the mask override signal is active regardless of whether the mask activation signal is enabled or disabled.

Petitioner asserts that Tokiwa discloses a second example where an interrupt is generated by VMCP interval timer 22 while VM is in direct execution mode (i.e., VM mode flag 13' is "1"). Pet. 14–15. Petitioner adds that in this mode, "the VMCP interval timer . . . always performs the interrupt, regardless of the contents of the interrupt masks (E and IT)." *Id.* (quoting Ex. 1002, 5). We understand Petitioner's position to be that VM mode flag 13 set to "1" discloses an override signal. Pet. 14. Based on the current record, we are persuaded that the alleged teachings in Tokiwa sufficiently meet this limitation.

Cancelled claim 4 depends from claim 1 and recites that the "mask override signal is enabled based on a hardware condition." Cancelled claim 5 depends from claim 4 and requires that the interrupt mask disable circuit is incorporated within a processor and "the hardware condition occurs when said processor is in a particular state." For these limitations, Petitioner relies on the VM mode and HPV mode for the required hardware condition and processor state. Pet. 15–17. Additionally, Petitioner points to Tokiwa's description of a virtual machine system having a VMCP that manages resources (central processing units, main memory devices, progress status words (PSWs), control registers, and input/output devices). *Id.* at 17.

Claim 6 depends from claim 5 and further requires the "particular state comprises an idle mode." For the "idle mode," Petitioner points to Smith's disclosure of an apparatus for inhibiting clock signals in response to a WAIT or STOP instruction. Pet. 17–19. Petitioner further asserts that Smith discloses an override that allows an interrupt to cause the processor to operate out of a low-power state, even if the interrupt is masked. *Id.* at 9–10. Petitioner also argues that "[a] person of ordinary skill in the art would have known that combining Smith's 'idle mode' circuitry within Tokiwa's interrupt mask disable circuitry would yield predictable, expected and beneficial results" of keeping a mask signal from preventing the processor from waking from an interrupt when in a low power state. *Id.* at 10.

Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on the assertion that claim 6 would have been obvious over Tokiwa and Smith. Further, Petitioner provides detailed explanations of how each limitation of claims 7–9 is taught or suggested by the combination of Tokiwa and Smith, which are persuasive

at this stage of the proceeding. Pet. 19–20. Thus, we are persuaded that Petitioner has demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 7–9 on this ground.

*C. Claims 6–9 – Obviousness Over Katayose and Smith*

Petitioner argues that claims 6–9 are unpatentable under 35 U.S.C. § 103 over Katayose and Smith. Pet. 7, 48–60. As explained in further detail below, we have considered the arguments and evidence presented, and conclude that Petitioner has established a reasonable likelihood of prevailing on this ground.

*1. Summary of Katayose (Ex. 1003)*

Katayose discloses a data processor with two different interrupt processing modes. Ex. 1003, 1:7–10. Katayose calls the first mode a "vector interrupt" mode and the second mode a "macroservice" mode. *Id.* at 3:6–7, 17–28. In the vector interrupt mode, vectors are assigned to peripheral devices and an interrupt circuit to specify a "head address of respective interrupt routines held in a program memory." *Id.* at 1:59–60. This allows selection of a program appropriate to the interrupt request from a plurality of interrupt processing programs. *Id.* at 1:52–60. In the macroservice mode, "if the interrupt request is generated, the execution of the current program is interrupted and an ordinary program execution operation of the CPU is stopped." *Id.* at 3:18–22.

Referring to Figure 1, Katayose describes interrupt controller 100, which includes interrupt request flag 102 and mode designation (MS/INT) Flag 104. Ex. 1003, 4:19–22. When a processing request is generated from a peripheral device and interrupt request flag 102 is set, controller 100 makes the INTRQ signal active and reads the content of the mode

designation flag 104 to make the MS/INT signal active or inactive. *Id.* at 4:52–57. When the MS/INT signal is low, execution unit 200 executes the vector interrupt. *Id.* at 4:63–65. When the MS/INT signal is high, interrupt processing occurs through macroservice mode. *Id.* at 5:11–13.

Figure 6, reproduced below, shows a logic circuit diagram for an interrupt controller. Ex. 1003, 3:65–66.

FIGURE 6

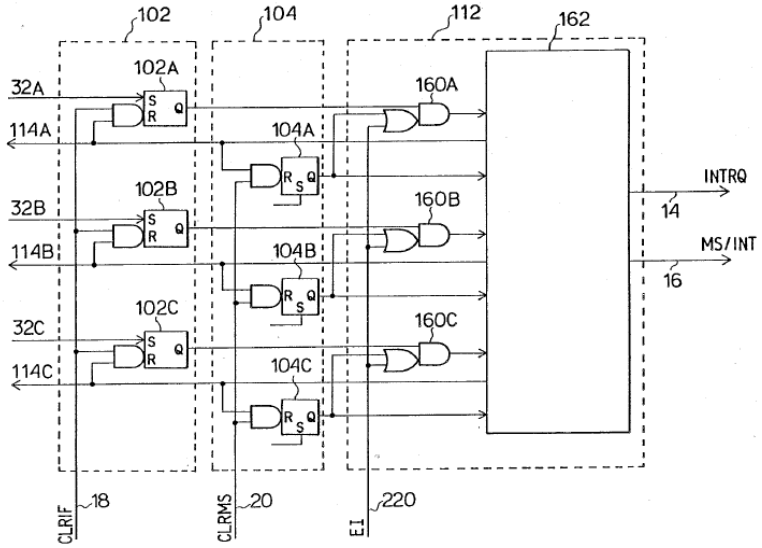



Figure 6's logic circuit diagram includes interrupt flag 102, mode designation flag 104, and interrupt processing circuit 112. Additionally, Figure 6 includes logic gates 160A, B, and C, which respectively receive interrupt request flags 102A, B, and C; mode designation flags 104A, B, and C; and an EI flag signal. Ex. 1003, 14:16–21. The EI flag signal is an interrupt enable flag that is set when an interrupt processing is allowed and is reset when an interrupt processing is already being executed or when an interrupt should be inhibited. *Id.* at 2:6–9.

When mode selection flag 104 is set (i.e., macroservice mode) and interrupt request flag 102A is set, AND-OR logic 160A generates a high level output regardless of the EI flag signal. Ex. 1003, 14:33–36. The execution unit detects that the INTRQ signal is set to high and the MS/INT signal is set to high, and executes macroservice. *Id.* at 14:50–52. In vector interrupt mode, mode designation flag 104 is reset and the MS/INT signal is low. If EI flag signal 220 is at a high level, the output of AND-OR gate 160A is high. *Id.* at 14:63–68. If EI flag signal 220 is low, the output of AND-OR logic 160A is brought to a low level and the AND-OR gate maintains its output at a low level regardless of the content of the corresponding interrupt request flag. *Id.* at 15:13–17.

*2. Analysis*

Below we discuss claim 6, which is illustrative of claims 7–9. Again, our discussion of claim 6 includes the limitations recited in cancelled claims 1, 4, and 5, which are required in dependent claim 6.

Cancelled claim 1 recites an interrupt mask disable circuit with

> first logic circuitry operably coupled to receive an interrupt request and a mask signal and to provide an interrupt signal when the interrupt request is active and the mask signal is disabled, and to provide a non-interrupt signal when the mask signal is enabled regardless of whether the interrupt request is active or inactive.

To meet this limitation, Petitioner asserts that Katayose discloses AND gates 160A, 160B, and 160C, which receive signals respectively from interrupt request flags 102A, 102B, and 102C and OR gates. Pet. 48; *see also id.* at 52–53 (claim chart). Petitioner adds that one of the signals from the OR gates is EI flag, which allows activation of a mask signal. *Id.* Based on the current record, we are persuaded by Petitioner's arguments.

Cancelled claim 1 further requires a

> second logic circuitry operably coupled to receive a mask activation signal and a mask override signal and to produce the mask signal, wherein the mask signal is enabled when the mask activation signal is active and the mask override signal is not enabled and wherein the mask signal is disabled when the mask override signal is active regardless of whether the mask activation signal is enabled or disabled.

Petitioner asserts that Katayose's mode selection flag 104 provides a mask override signal. Pet. 48; *see also id.* at 53–54 (claim chart). "When high, the mode selection flag 104 signal causes the output of the OR gate to be high, which will cause the interrupt to fire even if the EI flag is set to low (i.e., the interrupt is masked)." Pet. 48. We are persuaded by Petitioner's argument.

Cancelled claim 4 depends from claim 1 and recites that the "mask override signal is enabled based on a hardware condition." Cancelled claim 5 depends from claim 4 and requires that the interrupt mask disable circuit is incorporated within a processor and "the hardware condition occurs when said processor is in a particular state."

For these limitations, Petitioner asserts that Katayose discloses controller 100, which includes interrupt request flag 102 and mode designation flag 104. Pet. 55–56. Petitioner adds that Katayose describes a "third case" where the mode designation flag 104 is set for the macroservice mode and both the INTRQ and MS/INT signal are rendered active to a high level regardless of the content of EI flag 218. *Id.* at 54. We understand Petitioner's position to be that the macroservice mode meets the limitations of a hardware condition and processor state recited in cancelled claims 4 and 5. Based on the current record, we are persuaded by Petitioner's arguments.

Claim 6 depends from claim 5 and further requires the "particular state comprises an idle mode." For the "idle mode," Petitioner points to Smith's disclosure of an apparatus for inhibiting clock signals in response to a WAIT or STOP instruction. Pet. 58. Petitioner further asserts that Smith discloses receiving an INT signal after executing a STOP instruction, whereby flip-flop 148 is reset regardless of the state of the MASK1 signal. *Id.* at 22, 58–59. Petitioner asserts several reasons why one of ordinary skill in the art would have combined the alleged teachings in Katayose and Smith. *Id.* at 50–51. These reasons include that combining the different interrupt modes described in Katayose with the idle mode disclosed in Smith would reduce power consumption and "'provide an apparatus for disabling clock signals in an intelligent manner until further processor operations become necessary.'" *Id.* at 50 (citing Ex. 1004, 2:2–15).

Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on the assertion that claim 6 would have been obvious over Katayose and Smith. Further, Petitioner provides detailed explanations of how each limitation of claims 7–9 is taught or suggested by the combination of Katayose and Smith, which are persuasive at this stage of the proceeding. Pet. 59–60. Thus, we are persuaded that Petitioner also has demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 7–9 on this ground.

*D. Claims 6 and 7 – Anticipation by Smith (Ex. 1004)*

Petitioner argues that claims 6 and 7 are unpatentable under 35 U.S.C. § 102(b) over Smith. Pet. 20–29. Below, we discuss claim 6, which is illustrative of claim 7. Again, we begin our discussion with cancelled claims 1, 4, and 5, from which claim 6 depends.

Petitioner asserts that Smith's disclosure of basic interrupt masking functionality satisfies the first logic circuitry recited in claim 1. Specifically, Petitioner asserts Smith's fourth bit of the condition code register is a mask interrupt bit that when set disables external and timer interrupts, and clearing the interrupt mask bit enables interrupts. Pet. 21 (citing Ex. 1004, 3:24–25). Petitioner also refers to Smith's logic diagram depicted in Figure 4, which shows an INT signal and a MASK1 signal. *Id.* Smith discloses that in the WAIT mode, the presence of an INT signal and the absence of a MASK1 signal will result in a "logical '0' [that] is applied to the D input of flip-flop 148," Ex. 1004, 7:29–32, which then results in a logical "1" applied to the reset input of WAIT flip-flop 98, which enables clock signals C1 and C2 and address and data strobe signals AS and DS, *id.* at 7:43–48.

For the second logic circuitry recited in claim 1, Petitioner asserts Smith discloses the ability to wake from a STOP mode when an interrupt is received, regardless of the mask signal. Referring to Figure 4, Petitioner asserts that the STOP mode, indicated by a logical "1" on the STOP output of flip-flop 100, is fed into the reset path of interrupt flip-flop 148 via NAND gate 180 and inverter 184. Pet. 21–22. The INT signal (at "1" when indicating an interrupt) and inverted C2 clock signal ("0" in STOP mode) are also inputs to NAND gate 180. *Id.* at 22. Based on these inputs, Petitioner adds that flip-flop 148 will be reset to logical "0," regardless of the MASKI signal. *Id.*

We are persuaded by Petitioner's argument. Smith discloses that a received INT signal, the STOP signal, and inverted C2 clock signal are at "1" when input into NAND gate 180. Ex. 1004, 8:48–61. With these inputs, NAND gate 180 outputs 0, which is inverted by inverter 184 to a "1" and

applied to the R input into flip-flop 148 to reset flip-flop 148. Ex. 1004, 8:53–63.

Cancelled claim 4 depends from claim 1 and recites that the "mask override signal is enabled based on a hardware condition." Cancelled claim 5 depends from claim 4 and requires that the interrupt mask disable circuit is incorporated within a processor and "the hardware condition occurs when said processor is in a particular state." Claim 6 further recites that the particular state comprises an idle mode. Petitioner argues that Smith's apparatus operates in synchronization with clock signals generated by a master clock oscillator. Pet. 27–29. Thus, depending on the state of the master clock oscillator (e.g., STOP mode or WAIT mode), a mask override signal may be enabled. Petitioner further argues that the idle mode is disclosed by Smith's STOP mode. *Id.*

Based on the current record, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on the assertion that Smith discloses claim 6. Further, Petitioner provides detailed explanations of how each limitation of claim 7 is disclosed by Smith, which are persuasive at this stage of the proceeding. Pet. 29. Thus, we are persuaded that Petitioner also has demonstrated that there is a reasonable likelihood that it would prevail with respect to claim 7 on this ground.

*E. Other Grounds*

Petitioner asserts that claims 6 and 7 are unpatentable under 35 U.S.C. § 102(b) over OKI or NEC. Pet. 7. Additionally, Petitioner asserts that claims 6 and 7 are unpatentable under 35 U.S.C. § 103(a) over Smith. *Id.*

We determine that these grounds are redundant to the grounds of unpatentability on which we institute *inter partes* review for the same

claims, and exercise our discretion not to institute review on these grounds. *See* 37 C.F.R. § 42.108(a). Exercise of our discretion in declining to institute on the grounds based on OKI and NEC is consistent with the authority granted under 35 U.S.C. § 315(d) to manage *inter partes* proceedings and with the objective of "secur[ing] the just, speedy, and inexpensive resolution of every proceeding." 37 C.F.R. § 42.1.

## III. CONCLUSION

For the foregoing reasons, we are persuaded that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail with respect to claims 6–9.

The Board has not made a final determination on the patentability of any challenged claims.

## IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '597 patent is hereby instituted as to claims 6–9 for the following grounds:

A. Claims 6–9 as unpatentable under 35 U.S.C. § 103 over Tokiwa and Smith

B. Claims 6–9 as unpatentable under 35 U.S.C. § 103 over Katayose and Smith; and

C. Claims 6 and 7 as unpatentable under 35 U.S.C. § 102(b) over Smith;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial is commencing on the entry date of this decision; and

FURTHER ORDERED that the trial is limited to the grounds identified above and no other grounds are authorized.

PETITIONER:

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